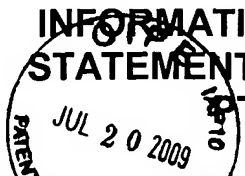


<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS</b> <b>PTO-1449</b> 	Attorney Docket No. 2885/86	Serial No. 10/501,845
	Applicant(s) Martin VORBACH et al.	
	Filing Date August 26, 2005	Group Art Unit 2183

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,686,386	08-11-1987	Tadao			
	5,287,532	02-15-1994	Hunt			
	5,412,795	05-02-1995	Larson			
	5,525,971	06-11-1996	Flynn			
	5,675,757	10-07-1997	Davidson et al.			
	5,694,602	12-02-1997	Smith			
	5,745,734	04-28-1998	Craft et al.			
	6,035,371	03-07-2000	Magloire			
	6,055,619	04-25-2000	North et al.			
	6,868,476	03-15-2005	Rosenbluth et al.			
	7,216,204	05-08-2007	Rosenbluth et al.			
	2001/0018733	08-30-2001	Fujii et al.			
	2002/0013861	01-31-2002	Adiletta et al.			
	2002/0124238	09-05-2002	Metzgen			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	198 22 776*	03-25-1999	DE				X
	1 115 204	07-11-2001	EP				X
	2 304 438	03-19-1997	GB				X
	00/045282	08-03-2000	WO				X
	03/091875	11-06-2003	WO				X
	01-229378*	09-13-1989	JP				X
	06-266605*	09-22-1994	JP				X
	07-086921*	03-31-1995	JP				X
	08-101761*	04-16-1996	JP				X
	08-102492*	04-16-1996	JP				X
	08-148989*	06-07-1996	JP				X

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/86	Serial No. 10/501,845
	Applicant(s) Martin VORBACH et al.	
	Filing Date August 26, 2005	Group Art Unit 2183

**FOREIGN DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	08-221164*	08-30-1996	JP				X
	09-294069*	11-11-1997	JP				X
	2000-076066*	03-14-2000	JP				X
	2000-311156*	11-07-2000	JP				X

\* English-language Abstract provided.

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Advanced RISC Machines, "Introduction to AMBA," Section 1, pp. 1-1 to 1-7 (October 1996)
	ARM, "The Architecture for the Digital World," <a href="http://www.arm.com/products">http://www.arm.com/products</a> , 3 pages (March 18, 2009)
	ARM, "The Architecture for the Digital World; Milestones," <a href="http://www.arm.com/aboutarm/milestones.html">http://www.arm.com/aboutarm/milestones.html</a> , 5 pages (March 18, 2009)
	Asari, et al., "FeRAM circuit technology for system on a chip," Proceedings First NASA/DoD Workshop on Evolvable Hardware, pp. 193-197 (1999)
	Cardoso, et al., "Compilation and Temporal Partitioning for a Coarse-Grain Reconfigurable Architecture," LYSACHT, P. & ROSENTIEL, W. eds., "New Algorithms, Architectures and Applications for Reconfigurable Computing," pp. 105-115 (2005)
	Cardoso, J.M.P. et al., "Macro-Based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," Field-Programmable Custom Computing Machines (1999) FCCM '99. Proceedings. Seventh Annual IEEE Symposium on NAPA Valley, CA, USA, 21-23 April 1999, IEEE Comput. Soc, US, (21 April 1999) pp.2-11
	Cook, "The Amalgam Compiler Infrastructure," Thesis at the University of Illinois at Urbana-Champaign, Ch. 7 & Appendix G (2004)
	Del Corso, et al., "Microcomputer Buses and Links," Academic Press Inc. Ltd., pp. 138-143, 277-285 (1986)
	Fawcett, "Map, Place and Route: The Key to High-Density PLD Implementation," Wescon Conference, IEEE Center, pp. 292-297 (7 November 1995)
	Hendrich, et al., "Silicon Compilation and Rapid Prototyping of Microprogrammed VLSI-Circuits with MIMOLA and SOLO 1400," Microprocessing & Microprogramming 35(1-5): 287-294 (1992)
	"IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE Std. 1149.1-1990, pp. 1-127 (1993)
	Jefferson, et al., U.S. Provisional Application Serial No. 60/109,417 filed November 18, 1998.
	Koch, et al., "High-Level-Language Compilation for Reconfigurable Computers," Proceedings of European Workshop on Reconfigurable Communication-Centric SOCS, 8 pages (2005)

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/86	Serial No. 10/501,845
	Applicant(s) Martin VORBACH et al.	
	Filing Date August 26, 2005	Group Art Unit 2183

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/	Lee, et al., "Multimedia extensions for general-purpose processors," IEEE Workshop on Signal Processing Systems, SIPS 97 – Design and Implementation, pp. 9-23 (1997)
	Mei, et al., "Adres: An Architecture with Tightly Coupled VLIW Processor and Coarse-Grained Reconfigurable Matrix," Proc. Field-Programmable Logic and Applications (FPL 03), Springer, pp. 61-70 (2003)
	Moraes, et al., "A Physical Synthesis Design Flow Based on Virtual Components," XV Conference on Design of Circuits and Integrated Systems, 6 pages (2000)
	Neumann, et al., "A Generic Library for Adaptive Computing Environments," Field Programmable Logic and Applications, 11 <sup>th</sup> International Conference, FPL 2001, Proceedings (Lecture Notes in Computer Science, vol. 2147), pp. 503-512 (2001)
	Ohmsha, "Information Processing Handbook," edited by the Information Processing Society of Japan, pp. 376, December 21, 1998.*
	PCI Local Bus Specification, Production Version, Revision 2.1, Portland, OR, pp. 1-281 (June 1, 1995)
	Pirsch, et al., "VLSI implementations of image and video multimedia processing systems," IEEE Transactions on Circuits and Systems for Video Technology 8(7): 878-891 (Nov. 1998)
	Salefski, et al., "Re-configurable computing in wireless," Annual ACM IEEE Design Automation Conference: Proceedings of the 38th conference on Design automation, pp. 178-183 (2001)
	Schönfeld, et al., "The LISA Design Environment for the Synthesis of Array Processors Including Memories for the Data Transfer and Fault Tolerance by Reconfiguration and Coding Techniques," J. VLSI Signal Processing Systems for Signal, Image, and Video Technology 11(1/2): 51-74 (1995)
	Schmidt, et al., "Datawave: A Single-Chip Multiprocessor for Video Applications," IEEE Micro 11(3): 22-25 and 88-94 (Jun. 1991)
	Shin, et al., "C-based Interactive RTL Design Methodology," Technical Report CECS-03-42, pp. 1-16 (2003)
	Sondervan, "Retiming and logic synthesis," Electronic Engineering 65(793): 33, 35-36 (1993)
	"The Programmable Logic Data Book," XILINX, Inc., Section 2, pp. 1-240, Section 8, pp. 1, 23-25, 29, 45-52, 169-172 (1994)

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	